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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Box Patent Application
Washington, D. C 20231

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) are the specification and claims of the nonprovisional patent application of:

Yoshinori UEDA for
Inventor

SEMICONDUCTOR DEVICE HAVING AN INTEGRAL RESISTANCE ELEMENT
Title of Invention

APPLICATION ELEMENTS ENCLOSED:

1. X Specification (total pages 26) including:
   a. 5 pages of claims (9 claims)
   b. 1 page Abstract
2. X 9 sheets of ___ informal X formal drawings (Figs. 1-6)
3. X Oath or declaration of Applicants (2 total pages)
   a X Newly executed (original or copy)
   b. ____ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Item 14 completed)
4. ____ Deletion of Inventor(s)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1 33(b)
5. ____ Incorporation By Reference
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied in item 3b is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ___ Microfiche Computer Program (Appendix)

APPLICATION PARTS ENCLOSED:

7. X An assignment of the invention to Ricoh Company, Ltd. (cover sheet & document(s))
8. ___ 37 CFR 3.73(b) Statement (*when there is an assignee*)
9. X Power of Attorney
   a. X Newly executed (original or copy)
   b. ____ Copy from a prior application

10._X_ Information Disclosure Statement (IDS)/PTO-1449

_X_ Copies of IDS Citations

11.___ A Preliminary Amendment

12._X_ Return Receipt Postcard (MPEP 503)

13.___ A small entity statement under 37 C.F.R. §1.9 and §1 27

____ Statement filed in prior application, status still proper and desired

14.___ If a Continuing Application, *check the appropriate box and supply the requisite information*:

☐ Continuation of prior application No.: __________ filed __________

☐ Divisional of prior application No.: __________ filed __________

☐ Continuation-in-part (CIP) of prior application No.: __________ filed __________

15.___ Amend the specification by inserting before the first line of page one: --This is a ___ continuation ____ divisional of application Serial No. ______ filed ____.--

16._X_ Priority of application No. 10-317265 filed in Japan on November 9, 1998. Applicant hereby claims priority under 35 U.S.C. § 119.

_X_ A certified copy of priority application No 10-317265 is enclosed

___ A certified copy of priority application No. _________ has been filed in prior application S.N. ____________ filed _____________

17.___ Other (identify) ____

The filing fee is calculated as follows:

CLAIMS AS FILED, LESS ANY CLAIMS CANCELLED BY AMENDMENT

					Rate			Fee	
	Number Filed		Number Extra*		Small Entity	Other Entity		Small Entity	Other Entity
Total Claims	9-20	=	0	x	$ 9	$ 18	=	$	$ 0
Indep. Claims	2-3	=	0	x	$ 39	$ 78	=	$	$ 0
Multiple Dependent Claims Presented: Yes____ No_X_					$130	$260	=	$	$ 0
If the difference in column 1 is less than zero, enter "0" in column 2					Basic Fee			$ 380	$ 760
					Total Fee				$ 760

18. X A check in the amount of $ 760.00 to cover the filing fee.

19. ___ Please charge Deposit Account No. 03-3125 in the amount of $ 40.00 for recordation of the Assignment.

20. X The Commissioner is hereby authorized to charge any additional fees which may be required in connection with the following or credit any overpayment to Deposit Account No. 03-3125.

- X Filing fees under 37 C.F.R. § 1.16.
- X Patent application processing fees under 37 C.F.R. §1.17.
- ___ The issue fee set in 37 C.F.R. §1.18 at or before mailing of the Notice of Allowance, pursuant to 37 C.F.R §1.311(b).

21. X Three copies of this sheet are enclosed.

22. ___ Other (identify) ______________________

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Dkt. 2271/60617

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of :	Yoshinori UEDA		
Serial No. :	Not Yet Assigned	Group Art Unit:	
Date Filed :	Concurrently Herewith	Examiner:	
For :	SEMICONDUCTOR DEVICE HAVING AN INTEGRAL RESISTANCE ELEMENT		

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Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

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Express Mail mailing label number: EM157609600US

Date of Deposit: November 1, 1999

I hereby certify that the above-identified application consisting of a 26-page specification, 9 claims, 9 sheets of formal drawings (Figs. 1-6), 3 copies of transmittal form, Information Disclosure Statement, Form PTO-1449 and copies of cited references, executed Declaration and Power of Attorney, 1595 Recordation Form, executed Assignment form, a certified copy of Japanese Patent Appln. No. 10-317265 filed November 9, 1998 and a check for $40.00 for Assignment fee, and check for $760 filing fee, is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

LIN ISCOA

Mail Room Employee
Depositing Express Mail Material

Attorney for Applicant:

IVAN S. KAVRUKOV, Reg. No. 25,161
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Tel: (212) 278-0400

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT I, YOSHINORI UEDA, a citizen of Japan residing at Hyogo, Japan have invented certain new and useful improvements in

SEMICONDUCTOR DEVICE HAVING AN INTEGRAL RESISTANCE ELEMENT

of which the following is a specification:-

BACKGROUND OF THE INVENTION

The present invention generally relates to semiconductor devices and more particularly to a semiconductor device having a resistance element and a fabrication process thereof.

The present invention covers not only a resistance element formed on a semiconductor chip, but also an integrated circuit in which such a resistance element is integrated on a common chip, together with other elements such as transistors and/or capacitors.

In semiconductor devices, resistance elements are formed generally by a patterning process of a polysilicon layer, wherein such a polysilicon layer may be formed on a diffusion region on a semiconductor substrate or on an insulation film covering the semiconductor substrate.

In order to minimize the variation of the resistance of such resistance elements, it has been practiced to minimize the sheet-resistance variation of the conductive layer from which the resistance pattern is formed. Alternatively, efforts are made to improve the precision of the patterning process.

In order to minimize the sheet-resistance variation of the conductive layer, various proposals have been made so far, including controlling of the

thickness of the conductive layer or improving the quality of the conductive layer. See the Japanese Laid-Open Patent Publication 7-115173 or 9-232521.

With regard to the approach via improvement of the patterning precision of the resistance elements, there is a proposal to planarize the polysilicon layer such that the precision of the patterning is improved. See the Japanese Laid-Open Patent Publication 5-218306. Further, there is a proposal to improve the patterning precision by disposing a dummy pattern adjacent to the resistance pattern. The present invention to be described later also adopts the approach to minimize the resistance variation by improving the precision of the resistance pattern elements.

According to the foregoing approach of improving the patterning precision of the resistance, on the other hand, it has been difficult to achieve a significant improvement with regard to the resistance variation, particularly when the size of the resistance element is small. Thus, in order to avoid the foregoing problem, it has been practiced to form the resistance elements to has a relatively large size such that the variation in the patterning of the resistance element can be ignored. Such an approach, on the other hand, reduces the area of the semiconductor chip on which

other elements such as transistors or interconnection patterns could otherwise have been formed. Thus, such an approach has caused an increase in the size and hence the cost of the semiconductor devices.

FIG.1 shows an example of such a polysilicon resistance element.

Referring to FIG.1, there is provided a number of polysilicon resistance patterns 2 on a surface of a substrate (not shown) in a parallel relationship with each other, wherein the resistance patterns 2 are connected in series by conductor patterns 4 also provided on the substrate to form a desired resistance element having a desired resistance value. In the example in which the polysilicon layer has a sheet resistance of 5Ω/□ and ten such resistance patterns 2, each having a width W of 1 μm and a length L of 100 μm, are connected in series, the resistance element thus formed shows a nominal resistance value of 5000 Ω (= 5 Ω/□ x (100 μm x 1 μm) x 10).

Thus, when the resistance patterns 2 are formed with a size tolerance of 0.1 μm, the resistance value of the resistance element may vary within a range of ±500Ω or ±10%. In order to reduce such a variation of the resistance in the resistance element, it has been necessary to increase the size W and/or L for each of

the resistance patterns 2. As noted already, however, such an approach causes a decrease in the area of the semiconductor chip on which other devices are formed.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a novel and useful semiconductor device having a resistance pattern and a fabrication process thereof wherein the foregoing problems are eliminated.

Another and more specific object of the present invention is to provide a semiconductor device having a resistance pattern wherein direct influence of the patterning precision of the resistance pattern on the resistance value of the resistance element is eliminated.

Another object of the present invention is to provide a semiconductor device, comprising:

a substrate; and

a resistance element formed on said substrate, said resistance pattern comprising:

a first resistance pattern provided on said substrate at a first level; and

a second resistance pattern provided adjacent to said second resistance pattern at a second level

lower than said first level, said second resistance pattern being connected in series to said first resistance pattern,

said second resistance pattern having an edge defined by said first resistance pattern.

Another object of the present invention is to provide a method of fabricating a semiconductor device, comprising the steps of:

forming a conductive layer on a Si layer;

patterning said conductive layer selectively with respect to said Si layer, to form a conductor pattern;

depositing a metal film on said Si layer such that said conductive film covers said conductor pattern and an exposed part of said Si layer exposed by said conductive film;

annealing said metal film to form a salicide pattern in correspondence to said conductive pattern as a first resistance pattern, said annealing step further forming a salicide pattern in said Si layer in correspondence to said exposed part of said Si layer as a second resistance pattern; and

forming a conductor pattern connecting said first resistance pattern and said second resistance pattern in series.

According to the present invention, the second resistance pattern, forming a complementary pattern with respect to the first resistance pattern, effectively compensates for any resistance change caused by the size variation occurred in the first resistance pattern, as the second resistance pattern is formed by a self-alignment process that uses the first resistance pattern as a self-alignment mask. When the width of the first resistance pattern is increased or decreased as a result of the error at the time of the patterning of the resistance pattern, for example, the width of the second resistance pattern decreases or increases correspondingly, and the change of the overall resistance of the resistance element, formed by the series connection of the first and second resistance patterns, is effectively avoided. Thereby, the resistance element can be formed to have a miniaturized size by using a high-resolution photolithographic patterning process, and the size of the semiconductor device can be reduced.

By forming the first resistance pattern by a polycide layer, it becomes possible to increase the sheet resistance as compared with the case of using a diffused silicide layer. The use of polycide is also advantageous when integrating a polysilicon capacitor

together with the semiconductor device.

In the case the second resistance pattern is formed in a semiconductor substrate in the form of a salicide (self-aligned silicide) pattern, it is preferable to control the doping of the semiconductor substrate such that the parasitic MOS transistor, formed in the semiconductor substrate by the foregoing first and second resistance patterns, has a threshold voltage exceeding the supply voltage used in the semiconductor device. By doing so, the resistance element can be used in the semiconductor device without restricting the voltage appearing across the resistance element.

Other objects and further features of the present invention will become apparent from the following detailed description when read in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a diagram showing the construction of a conventional resistance element in a plan view;

FIGS.2A - 2K are diagrams showing the fabrication process of a resistance element according to a first embodiment of the present invention;

FIG.3 is a diagram showing the construction of the resistance element of the first embodiment in a plan

view;

FIG.4 is a diagram showing the effect of the resistance element of the first embodiment in comparison with the prior art;

FIGS.5A and 5B are diagrams showing the fabrication process of a resistance element according to a second embodiment of the present invention; and

FIG.6 is a diagram showing the construction of the resistance element of the second embodiment in a plan view.

DETAILED DESCRIPTION OF THE INVENTION

[FIRST EMBODIMENT]

FIGS.2A and 2B show the fabrication process of a semiconductor device according to a first embodiment of the present invention.

Referring to FIG.2A, a field oxide film 12 is formed on a Si substrate 10 of the p-type by a LOCOS process with a thickness of about 450nm, such that the field oxide film 12 defines a region on which a resistance element is to be formed. Although not illustrated, the field oxide film 12 also defines a region, on the Si substrate 10, in which a transistor is to be formed.

Next, in the step of FIG.2B, an ion

implantation process of B^+ is conducted under an acceleration voltage of 10 keV with a dose of 2 x $10^{14}cm^{-2}$, for example, into the active region defined in the step of FIG.2A, such that there occurs no turning-on of a parasitic MOS transistor which is formed in the active region as a result of formation of the resistance element, even in such a case a voltage equivalent to the supply voltage appears across the resistance element to be formed.

Next, in the step of FIG.2C, an oxide film 14 is formed on the surface of the active region by conducting a wet oxidation process at 850°C for 15 minutes, wherein the wet oxidation process thus forming the oxide film 14 induces a simultaneous formation of a gate oxide film in correspondence to the part of the substrate where the transistor is to be formed.

After the formation of the oxide film 14, a polysilicon film 16 is deposited in the step of FIG.2D on the structure of FIG.2C with a thickness of about 150 nm, followed by a photolithographic patterning process of the polysilicon film 16 and further the underlying oxide film 14, to form a number of polysilicon patterns 16A extending parallel with each other as represented in FIG.2E. As a consequence of the patterning of the polysilicon film 16 and the underlying oxide film 14,

the surface of the Si substrate 10 is exposed at a region 10A located between adjacent polysilicon patterns 16A.

Simultaneously to the step of FIG.2E, it should be noted that a gate electrode is formed outside the region of the substrate 10 on which the resistance element is formed, as a result of the patterning of the polysilicon film 16. As represented in FIG.2F showing the region of the substrate 10 on which a MOS transistor is to be formed, it can be seen that a gate oxide film 14G and a gate electrode 16G are formed as a result of the patterning process of the oxide film 14 and the polysilicon film 16. In the step of FIG.2F, it can be seen that diffusion regions 10B are formed in the substrate adjacent to the gate electrode 16G while using the gate electrode 16G as a self-alignment mask. As a consequence of forming the gate electrode 16G and the polysilicon pattern 16A from the common polysilicon film 16, the semiconductor device of the present embodiment has a structural feature such that the composition, including the impurity concentration level, of the polysilicon pattern 16A is identical with the composition of the gate electrode 16G.

Next, in the step of FIG.2G, a metal film 18 such as Ti, Co or W is deposited on the structure of

FIG.2E such that the metal film 18 covers the polysilicon patterns 16A and further the exposed regions 10A of the substrate 10.

Next, a thermal annealing process is applied in the step of FIG.2H to form a polycide region 20A on each of the polysilicon patterns 16A and simultaneously a salicide region 20B on the Si substrate 10 in correspondence to the foregoing exposed region 10A. The polycide region 20A and the underlying polysilicon pattern 16A form together a polycide pattern 19. It should be noted that each salicide region 20B thus formed in correspondence to the exposed region 10A is defined by the edges of the adjacent polycide patterns 19. In other words, the salicide region 20B is formed in a self-aligned relationship with respect to the adjacent polycide patterns 19.

Next, in the step of FIG.2I, an insulation film 21 is provided on the structure of FIG.2H so as to cover the polycide patterns 19 and further the salicide regions 20B, and contact holes 22 and 24 are formed in the insulation film 21 in the step of FIG.2J so as to expose the polycide patterns 19 and the salicide regions 20B, respectively.

Finally, in the step of FIG.2K, local interconnection patterns 26 of Al or Ti is provided on

the insulation film 21 so as to connect a polycide pattern 19 to a corresponding salicide region 20B.

As a result of the step of FIG.2J, a structure represented in FIG.3 is obtained, wherein it can be seen that the polycide patterns 19 and the adjacent salicide regions 20B are connected at the contact holes 22 and 24 formed at respective ends thereof by the local interconnection patterns 26, to form a resistance element in which the polycide patterns 19 and the salicide regions 20B are connected in series.

As can be seen in FIG.3, the polycide patterns 19, each having a width W and a length L, are arranged in a parallel relationship with each other with a mutual separation S. Thereby, it can be seen that the salicide regions 20B are between adjacent polycide patterns 19 with a width S and the same length L. Thus, when the width W of the polycide patterns 19 is increased or decreased, the width S of the salicide region 20B is decreased or increased, and the variation of the total resistance of the resistance element, caused as a result of the size variation of the polycide patterns 19, is effectively compensated for.

FIG.4 shows the resistance variation of the resistance element of FIG.3 as a function of the size variation of the polycide patterns 19.

Referring to FIG.4 showing the resistance *f* of the resistance element including five polycide patterns 19 each having the nominal width W of 1 μm and the length L of 100 μm and five salicide regions 20B each having the nominal width S of 1 μm and the length L of 100 μm, it can be seen that the resistance *f* is represented as a function of the size variation x with regard to the width W by a parabolic curve of which formula is given as

$$\begin{aligned} f(x) &= 2500/(1 + x) + 2500/(1 - x) \\ &= 5000/(1 + x)(1 - x), \end{aligned}$$

wherein it is assumed that both of the polycide pattern 19 and the salicide region 20B have a sheet resistance of 5 $\Omega/\square$ and that the size variation with regard to the length L is ignorable.

For the sake of comparison, FIG.4 also shows the corresponding resistance variation of the conventional resistance element of FIG.1 by a broken line.

As can be seen clearly from FIG.4, the resistance variation for the resistance element of FIG.3 is reduced to ±50 Ω when the polycide patterns 19 are formed with a patterning precision of ±0.1 μm, while the

magnitude of this resistance variation is smaller than the conventional case by the factor of 10 for the same patterning precision.

As explained before, this improvement is obtained due to the fact that each salicide region 20B is formed in a self-aligned relationship with respect to the polycide patterns 19 such that each salicide region 20B is defined by the edges of the adjacent polycide patterns 19. Thus, when the width W of the polycide pattern 19 is increased by +x μm, then the width S of the salicide region 20B is reduced by -x μm. When the width W is decreased by - x μm, on the other hand, the width S of the salicide region 20B is increased by +x μm. This self-compensation of the resistance variation appears most conspicuously when the polycide patterns 19 and the salicide regions 20B have generally the same resistance value.

As noted already with reference to FIG.2B, the active region on which the resistance pattern is formed is doped with B, such that the threshold voltage of the parasitic MOS transistor, formed in the active region of the Si substrate 10 by the polycide pattern 19 acting as the gate electrode and the adjacent salicide regions 20B acting as the source and drain regions, exceeds the supply voltage of the semiconductor device. By doing

so, turning-on of the parasitic MOS transistor is positively avoided even in such a case a voltage corresponding to the supply voltage appears across the resistance element.

[SECOND EMBODIMENT]

FIGS.5A and 5B show the fabrication process of a semiconductor device, particularly the part including a resistance element, according to a second embodiment of the present invention, wherein those parts corresponding to the parts described previously are designated by the same reference numerals and the description thereof will be omitted.

Referring to FIG.5A, a polysilicon film 30 is formed on the field oxide film 12 on the Si substrate 10 by a CVD process, with little or no impurity element added thereto, such that the polysilicon film 30 has a sheet resistance of 1×10^6 $\Omega/\square$ or more.

Further, an insulation film 32, which may be an SiO_2 film or an SiN film, is deposited on the substrate 10 so as to cover the polysilicon film 30 with a thickness such that no substantial breakdown occurs in the insulation film 32 even when a supply voltage is applied across the insulation film 32. In the case a supply voltage of 5 V is used, the insulation film 32 is

formed to have a thickness of preferably larger than 15 nm. Further, a polysilicon film 34 is deposited on the insulation film 32 by a CVD process, wherein the polysilicon film 34 may have a composition identical with the composition of the lower polysilicon film 30. Alternatively, the polysilicon film 34 may contain a larger amount of impurity element.

Next, in the step of FIG.5B, the upper polysilicon film 34 and the insulation film 32 are subjected to a photolithographic patterning process to form a number of polysilicon patterns 34a such that the polysilicon patterns 34a extend parallel with each other with a mutual separation, such that the lower polysilicon film 30 is exposed between adjacent polysilicon patterns 34a. After patterning the polysilicon patterns 34a, an ion implantation process of an impurity element such as As^+ is conducted under an acceleration energy of 40 keV with a dose of $5 \times 10^{15} cm^{-2}$, for example, and provide an electrical conductivity to the surface part of the polysilicon patterns 34a and further the surface part of the exposed part of the polysilicon film 30.

Further, a metal film of Co, Ti or W is deposited on the structure thus formed with a thickness of about 60 nm, such that the metal film covers each of

the polysilicon patterns 34a and further the exposed part of the lower polysilicon film 30. By applying a thermal annealing process to the structure thus obtained, a polycide region 36 is formed on each of the polysilicon patterns 34a. Further, a polycide region 38 is formed on the exposed part of the polysilicon film 30, wherein it will be noted that the polycide region 38 is formed in a self-alignment process that uses the polysilicon pattern 34a as a self-alignment mask. See the structure of FIG.5B, wherein FIG.5B represents the state in which the unreacted metal film is removed by an etching process. Thereby, the polycide region 36 and the underlying polysilicon pattern 34a form together a polycide pattern 37. Further, the polycide region 38 forms a polycide pattern 39.

Further, by providing a protective insulation film (not shown) on the structure of FIG.5B and connecting an end part of the polycide pattern 37 and an end part of the polycide pattern 39 by a local interconnection pattern 44 as represented in FIG.6, the polycide patterns 37 and the polycide patterns 39 are connected in series to form the desired resistance element. It should be noted that FIG.6 shows resistance element in a plan view, wherein it can be seen that the local interconnection pattern 44 is connected to the

polycide pattern 37 at a contact hole 40 formed in the protective insulation film and further to the polycide pattern 39 at a contact hole 42 formed also in the protective insulation film.

As the polycide pattern 39 is formed in a self-aligned relationship with respect to the polycide pattern 37, the increase in the width W of the polycide pattern 39 causes a corresponding decrease in the width S of the polycide pattern 39, and the variation of the total resistance of the resistance element is effectively compensated for, even in such a case the patterning process for patterning the polycide pattern 37 is conducted with an error, similarly to the case of FIG.4.

In the present embodiment, it should be noted that the polysilicon pattern 34 may also constitute a gate electrode of a MOS transistor in the region outside the field oxide film 12. In such a case, the patterning of the gate electrode and the patterning of the polysilicon patterns 34a are conducted simultaneously. Thus, in the case a side-wall oxide film is to be formed at both side walls of the gate electrode in relation to the formation of the LDD (lightly doped drain) structure in the MOS transistor, similar side-wall oxide films are formed also on the side walls of the polysilicon pattern

34a as a result of the deposition and etch-back of an oxide film.

Further, the present invention is not limited to the embodiments described heretofore, but various variations and modifications may be made without departing from the scope of the invention.

WHAT IS CLAIMED IS

1. A semiconductor device, comprising:

a Si substrate; and

a resistance element formed on said Si substrate,

said resistance pattern comprising:

a first resistance pattern provided on said substrate at a first level; and

a second resistance pattern provided adjacent to said second resistance pattern at a second level lower than said first level, said second resistance pattern being connected in series to said first resistance pattern,

said second resistance pattern having an edge defined by said first resistance pattern.

2. A semiconductor device as claimed in claim 1, wherein said resistance element further includes an

interlayer insulation pattern underneath said first resistance pattern with a shape in conformity with a shape of said first resistance pattern, said second resistance pattern being provided at a level lower than said interlayer insulation pattern.

3. A semiconductor device as claimed in claim 1, wherein said first resistance pattern includes a polysilicon pattern and a polycide region formed on said polysilicon pattern, said semiconductor device further comprising a MOS transistor having a polysilicon gate electrode having a composition substantially identical with a composition of said polysilicon pattern.

4. A semiconductor device as claimed in claim 1, wherein said first resistance pattern and said second resistance pattern have a substantially identical resistance.

5. A semiconductor device as claimed in claim 3, wherein said second resistance pattern is formed in said Si substrate in the form of a salicide region defined by said first resistance pattern.

6. A semiconductor device as claimed in claim 5, wherein said Si substrate includes an impurity element with a concentration level such that a parasitic MOS transistor, formed of said first resistance pattern acting as a gate electrode and a pair of said second resistance patterns at both lateral side of said first resistance pattern acting as source and drain regions, has a threshold voltage larger than a supply voltage used in said semiconductor device.

7. A semiconductor device as claimed in claim 1, wherein said second resistance pattern is formed on a device isolation film covering said substrate, said second resistance pattern including a first polysilicon

pattern provided on said insulation film and a salicide region formed on a surface part of said first polysilicon pattern defined by said first resistance pattern.

8. A semiconductor device as claimed in claim 7, wherein said first resistance pattern includes a second polysilicon pattern and a polycide region formed on said second polysilicon pattern, said second polysilicon pattern having an impurity concentration level substantially larger than an impurity concentration level of said first polysilicon pattern.

9. A method of fabricating a semiconductor device, comprising the steps of:

forming a conductive layer on a Si layer;

patterning said conductive layer selectively with respect to said Si layer, to form a conductor pattern;

depositing a metal film on said Si layer such that said conductive film covers said conductor pattern and an exposed part of said Si layer exposed by said conductive film;

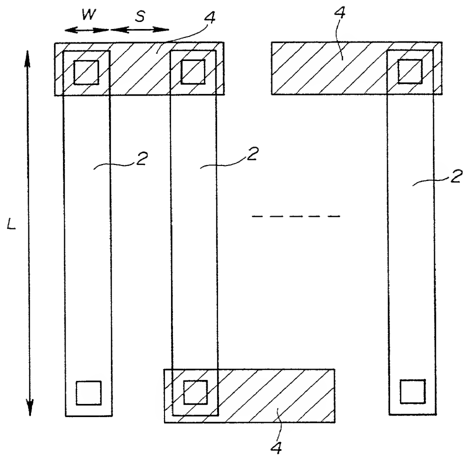
annealing said metal film to form a salicide pattern in correspondence to said conductive pattern as a first resistance pattern, said annealing step further forming a salicide pattern in said Si layer in correspondence to said exposed part of said Si layer as a second resistance pattern; and

forming a conductor pattern connecting said first resistance pattern and said second resistance pattern in series.

ABSTRACT OF THE DISCLOSURE

A resistance element of a semiconductor device includes a first resistance pattern and a second resistance pattern formed adjacent to the first resistance pattern at a lower level, wherein the second resistance pattern is defined by the first resistance pattern in a self-aligned relationship and connected to the first resistance pattern in series.

FIG. 1



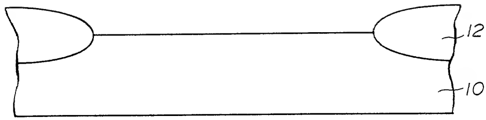


FIG. 2A

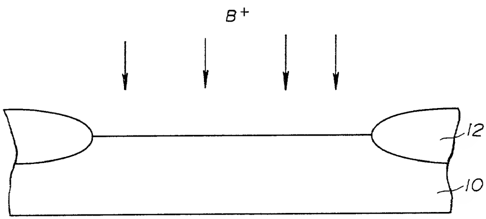


FIG. 2B

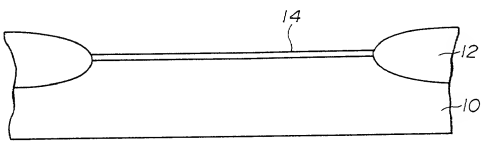


FIG. 2C

FIG.2D

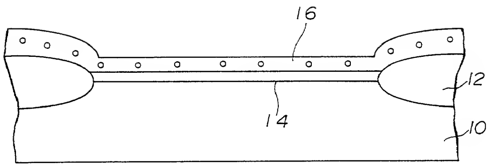


FIG.2E

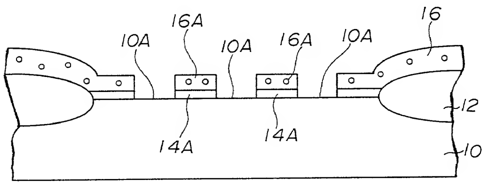


FIG.2F

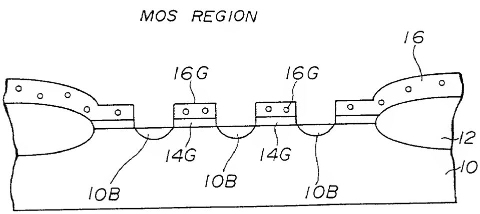


FIG. 2G

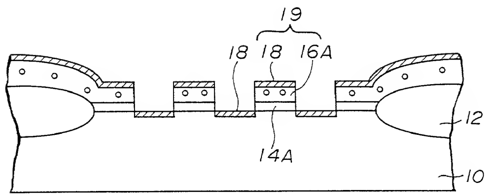


FIG. 2H

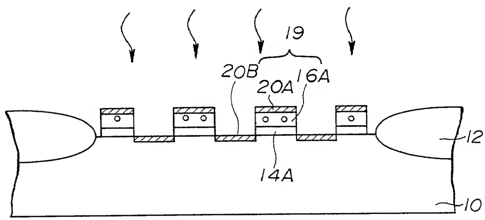


FIG. 2I

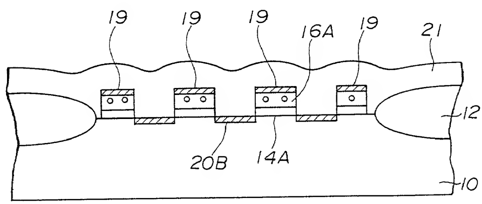
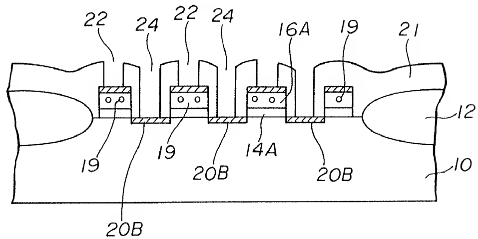
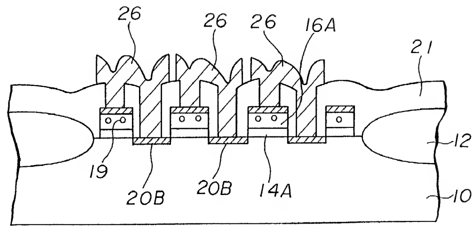


FIG.2J



22
24
22
24
16A
19
21
12
10
19
19
20B
14A
20B
20B

FIG.2K



26
26
26
16A
21
12
10
19
20B
20B
14A

FIG. 3

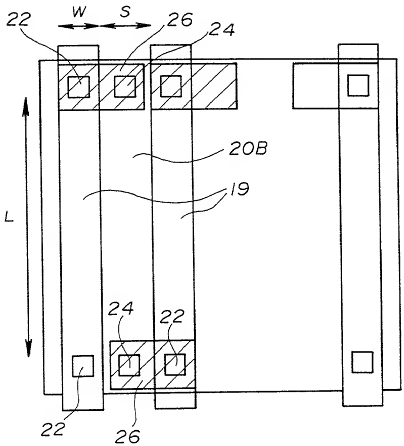


FIG.4

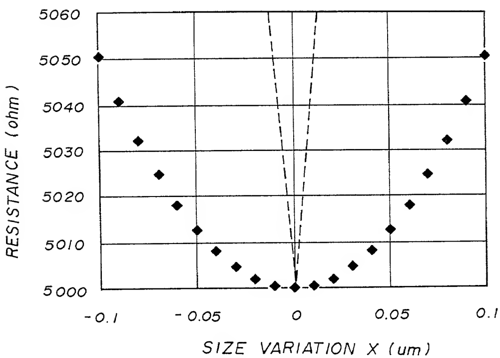

5060
5050
5040
5030
5020
5010
5000
RESISTANCE (ohm)
-0.1
-0.05
0
0.05
0.1
SIZE VARIATION X (um)

FIG.5A

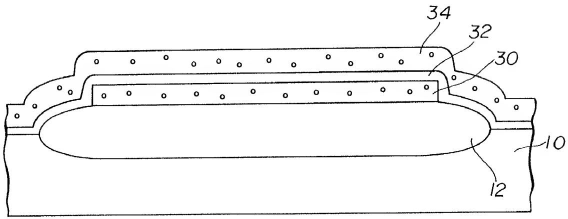


FIG.5B

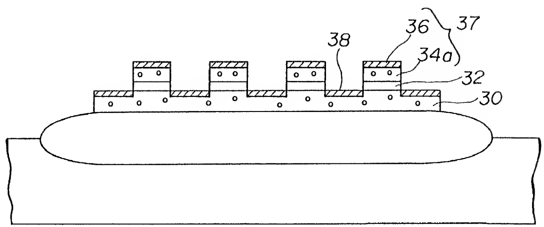
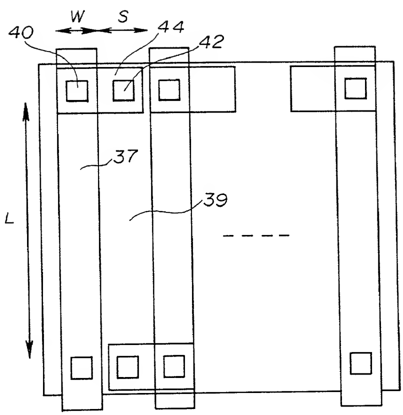


FIG. 6



DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR DEVICE HAVING AN INTEGRAL RESISTANCE ELEMENT

(Title of Invention)

the specification of which:
(check one)

X *is attached hereto.*

___ *was filed on* ____________

Application Serial No. ____________

and was amended by ____________.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) — *Priority Claimed*

Number	*Country*	*Filing Date*	*Yes*	*No*
Patent Application No.10-317265	Japan	9/November/1998	X	

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States Application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status

*And I hereby appoint **Ivan S. Kavrukov (Reg. No. 25161), Thomas F. Moran (Reg. No. 16579; Christopher C. Dunham (Reg. No. 22031); Norman H. Zivin (Reg. No. 25385), John P. White (Reg. No. 28678); Robert D. Katz (Reg. No. 30141); Peter J. Phillips (Reg. No. 29691); Richard S. Milner (Reg. No. 33970); Gerard M. Wissing (Reg. No. 36309); Richard F. Jaworski (Reg. No. 33515); and George M. Macdonald (Reg. No. 39284)** and each of them, all c/o Cooper & Dunham LLP of 1185 Avenue of the Americas, New York, New York 10036 (Tel. 212-278-0400), my attorneys, each with full power of substitution and revocation, to prosecute this application, to make alterations and amendments therein, to receive the patent, to transact all business in the Patent and Trademark Office connected herewith and to file any International Applications which are based thereon under the provisions of the Patent Cooperation Treaty.*

Please address all communications, and direct all telephone calls, regarding this application to:

Ivan S. Kavrukov *Reg. No.* ***25161***

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1185 Avenue of the Americas
New York, New York 10036
Tel. (212) 278-0400

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first joint inventor YOSHINORI UEDA

Inventor's signature Yoshinori Ueda

Citizenship Japan *Date of signature* Oct 13, 1999

Residence Hyogo, Japan

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